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LIGHTNING ACQUISITION AND BASIC TRIGGERING USING KINTEX-7 FPGA

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ABSTRACT

In this paper, the basic continuous acquisition of a Lightning signal at the rate of 1 MS/sec has been performed , as well as the time stamping of the acquired signal using the GPS module has been performed on the Lightning Sensor Node. The time stamping has been carried out to determine the Lightning location using the 'Time of Arrival' Technique in the further Sferic detection algorithms. The entire implementation has been carried out in real time using the cRIO-9030 controller. The process of data acquisition as well as the time stamping using the GPS module has been carried out on the Kintex-7 FPGA . The cRIO is used to handle the communication to the PC using an Ethernet. Further a triggering algorithm has also been implemented based on Amplitude thresholding on the FPGA. The implementation details along with the obtained results have been summarized in this paper.

Keywords - Sferic, FPGA to RT DMA FIFO, Kintex-7 FPGA, Cloud to Ground Lightning, cRIO, Network Streams

1. Introduction

This paper primarily focuses on the acquisition of the negative Cloud to Ground Lightning and development of the Digital Section of the Lightning Sensor Node. The Lightning Sensor Node currently has a Cross Magnetic Loop Antenna developed by [6] and a 'B' field analog front end of the lightning receiver developed by [5]. In this paper the focus is on the

implementation of the data acquisition along with the triggering algorithm. The triggering is based on the threshold value which is determined by the noise level at the site location, this threshold parameter has been used as an input to trigger the data acquisition. The acquisition in the currently developed system is a continuous data acquisition and all the buffers and memory elements have been efficiently handled on the FPGA as well as the cRIO controller, as a result there is no data loss while acquiring the data values and the time stamps from the FPGA .

The data acquired in real time from the FPGA can then in future be used to trigger the further Sferic processing blocks on the FPGA . The further Sferic processing algorithms would then be applied on the FPGA and the final confirmed data would then be transmitted in the form of frames from the FPGA to the cRIO and later to the PC using Network Streams .Ethernet has been used to transmit data from the cRIO to the PC . This paper focuses on the Data Acquisition, Time Stamping and the triggering algorithm which have been implemented on the FPGA . The paper also shows the communication of the data from the cRIO to the PC, as all the data points have been logged on the PC using the TDMS file format.

2. Design Architecture

This section explains the design details for the implementation which has been carried out on the FPGA. The design details have already been explained in detail in [1][2]. The important tasks which have been identified for the current implementation on the FPGA are as follows: Data Acquisition and Time stamping on the FPGA, Triggering algorithm based on the Amplitude Thresholding carried out on the FPGA. The design details for the current implementation on the cRIO has been discussed in detail by [1][2] .The cRIO has been used to only reconstruct the data and transfer the live data to the PC using Ethernet. The PC is used to store the data points along with the time stamps and also the live data has been plotted on the PC using Graph indicators in Labview . The implementation details for the basic triggering logic has been shown in the below flow chart.

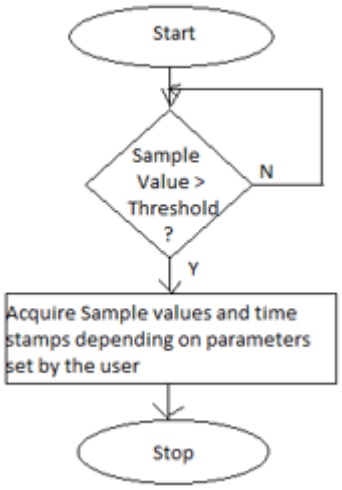

FIG 2.1. FLOW CHART FOR BASIC TRIGGERING

2.1 Significance Of Basic Triggering

The current implementation is used to acquire data continuously for long period of time . The triggering based on the noise level is the very first step to trigger the acquisition . In this case it's a very efficient technique to optimize the resources on the FPGA since the data is not continuously transmitted, as the threshold is being checked continuously prior to transmitting the data . In case of a negative lightning event , if the data lies below the threshold for a long time the FPGA does not waste its resources to buffer the unwanted data and transmit , it still checks once the data goes above threshold atleast once and in such cases the acquisition is being triggered and the data according to the number of data points to be acquired along with the relevant time stamp is being transmitted from the FPGA to the cRIO using FPGA to RT DMA FIFO . This helps in removal of the unwanted data at an early step of the Sferic detection.

3. Results and Discussion

The lightning signal is a pulse train[8] , due to the current climatic situation this pulse train was generated using a set of available hardware components as discussed in [1]. The generated pulse train is as shown in Fig. 3.1

FIG 3.1. GENERATED PULSE TRAIN

The pulse train shown in Fig 3.1 has been fed as an input to the channel 0 of the NI 9223 ADC module using the BNC connector . The Fig 3.1 shows the pulse train plot as observed on the Digital Storage Oscilloscope. The Front panel controls on the FPGA used to carry out the Basic Triggering algorithm has been shown in Fig 3.2

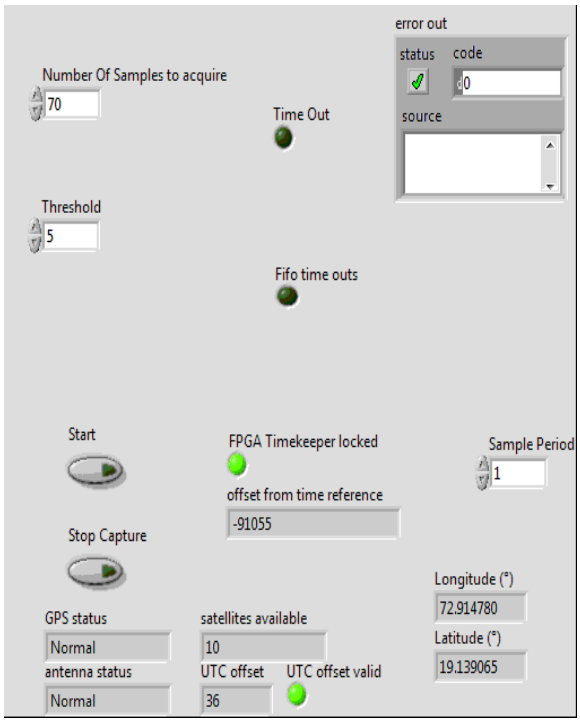

FIG 3.2. FRONT PANEL CONTROLS ON THE FPGA- BASIC TRIGGERING

In the above Front Panel the control parameters are the 'Number Of Samples to acquire', 'Threshold' and the 'Sample Period'. The Acquisition is triggered by pressing the Start button once the 'FPGA Timekeeper Locked' Led has been lit up . The acquisition can be stopped by pressing the 'Stop Capture' button.

The results obtained after applying the basic triggering logic , as observed on the PC is shown in Fig.3.3

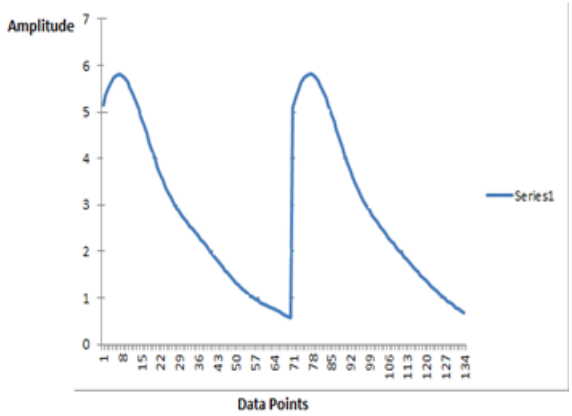

FIG 3.3. GRAPHICAL PLOT OF DATA CAPTURED ON THE PC

The Fig.3.3 shows the graphical plot of the data logged on the PC in a TDMS file format. The data values along with the time stamps logged on the PC is shown in Table 3.1

TABLE 3.1: LOGGED DATA VALUES AND TIME STAMPS

5.15299987	18:39 447778us
5.35415649	18:39 447779us
5.518127441	18:39 447780us
5.647171021	18:39 447781us
5.736434937	18:39 447782us
5.787857056	18:39 447783us
5.80305481	18:39 447784us

The Table 3.1 shows the logged values and the timestamps after converting it into UTC. In Fig 3.2 , the control parameters set on the FPGA show that the threshold has been set to 5 and the Number of

Samples to acquire has been set to 70 , which indicates that the signal is triggered if its amplitude exceeds 5 volt and post trigger seventy samples are to be acquired which is equivalent to a data of seventy microseconds, considering the situation that data is time stamped in microseconds. The electromagnetic signature of lightning has already been captured by *Haddad et.al.* [7]. The characteristic also includes the pulse width of the negative Cloud to Ground lightning signal. This can be used as a reference to set the Number of

Samples to acquire and this parameter would be in microseconds as each sample is acquired with a microseconds time stamp, after the threshold has been crossed. The implementation of the algorithm is clear from Fig 3.3 where the acquisition is triggered once the 5 V is crossed and later seventy data points are acquired as shown in Fig 3.2 and observation from the plot .The system again waits till the next threshold is crossed once again the acquisition has been triggered and later seventy data points have been acquired. Since the number of Samples to acquire has been set to seventy by the user, however, it can be set to any value depending on the total pulse width of the typical negative Cloud to Ground Lightning.

3.1 Advantages of the implemented basic Triggering algorithm

The significance of the triggering algorithm is efficient data acquisition for long period of time because the system waits till the trigger point is crossed before acquiring the sample values along with the time stamp. This helps in efficient data acquisition as there is no storage of data on the FPGA . Hence, there is no buffer overflow on the FPGA[3][4].This leads to efficient usage of the memory and also allows data logging for longer period of time. The limited data can now be sent to the further Sferic processing blocks on the FPGA to implement the further Sferic processing algorithms in order to determine the data as a valid lightning data chunk.

4. Conclusion

The current implementation is able to acquire the negative Cloud to Ground lightning within a frequency range of 3 – 30 Khz . The basic triggering algorithm which has been applied is based on the

threshold value set by the user. The threshold value is currently a user defined parameter .This parameter can be made adaptable by implementing the adaptable threshold value by averaging the sample values when the signal stays below the threshold. The current analog section of the Sensor Node is designed to work within a frequency range of 3-30 Khz[5]. The system can be made adaptable in future to work at 1 Mhz frequency, also the digital section can be implemented with the sampling rate of atleast 10 MS/sec, in order to accurately represent the sharp rise times and signal transitions of a Cloud to Ground Lightning signal.

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