# BRIDGELESS SEPIC POWER FACTOR CORRECTION RECTIFIER

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## ABSTRACT

*In this paper, the Single Ended Primary Inductor converter (SEPIC) is used to achieve high power factor with reduced input current ripple. The conventional power factor correction suffers from high conduction losses due to the diode bridge at the input side. Thus bridgeless SEPIC converter is used to avoid conduction loss by using only two semiconductor switches in the current flowing path during each switching cycle. By implementing the improved topology in DCM it ensures almost unity power factor in a simple and effective manner.*

**KEYWORDS:** Discontinuous Conduction Mode (DCM), Power Factor Correction (PFC), Single Ended Primary Inductance Converter (SEPIC).

## 1. Introduction

SEPIC is a DC/DC converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. This type of conversion is simple when the designer uses voltages from an unregulated input power supply. Hence this is very much preferred in applications such as battery chargers, power electronic circuits, home appliances, aircraft due to its less electromagnetic interference, inherent inrush current, reduced noise disturbances and less switching losses. The SEPIC topology is difficult to understand and requires two inductors, making the power-supply quite large.

Most of the presented bridgeless topologies so far [1]–[9] implement a boost-type circuit configuration (also referred to as dual-boost PFC rectifiers) because of its low cost and its high performance in terms of efficiency, power factor, and simplicity. These features have led power supply companies to start looking for bridgeless PFC circuit topologies. In [7], a systematic

review of the bridgeless PFC boost rectifier implementations that have received the most attention is presented along with their performance comparison with the conventional PFC boost rectifier. The bridgeless boost rectifier has the same major practical drawbacks as the conventional boost converter, such that the dc output voltage is always higher than the peak input voltage, input–output isolation cannot easily be implemented, the starting inrush current is high, and there is a lack of current limiting during overload conditions. Moreover, it is well known that the boost converter operating in discontinuous current mode (DCM) can offer a number of advantages such as inherent PFC function, very simple control, soft turn-on of the main switch, and reduced diode reversed-recovery losses. However, the DCM operation requires a high-quality boost inductor since it must switch extremely high peak ripple currents and voltages. As a result, a more robust input filter must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. The operation of SEPIC is similar to the bridgeless buck-boost PFC converter which has only three conducting semiconductors at every moment [1]. Comparing with the cascade buck-boost CBB-PFC converter, the efficiency is increased. Power factor is more than 0.98, and total harmonic distortion (THD) is less than one. The main features of the presented converter include high efficiency, low voltage stress on the semiconductor devices, and simplicity of design. These advantages are desirable features for high-power and high-voltage applications. The study of Bridgeless SEPIC Power Factor Correction rectifier under Discontinuous Conduction Mode is presented.

## 2. Bridgeless SEPIC PFC Rectifier

The bridgeless PFC circuits based on SEPIC with low conduction losses, is shown in Fig 1. Unlike the boost converter, the SEPIC converters offer several advantages in PFC applications, such as easy implementation of transformer isolation, inherent inrush current limitation during start-up and overload conditions, lower input current ripple, and less electromagnetic interference (EMI) associated with the DCM topology.

The topologies in Figure 1are formed by connecting two DC–DC SEPIC Converter one for each half-line period of the input voltage The operational circuits during positive and negative half-line period for the proposed bridgeless SEPIC rectifier of Fig.1 is shown respectively. Note that,

by referring to Fig.1 there are one or two semiconductors in the current flowing path. Each of the rectifier utilizes two power switches ($Q_1$ and $Q_2$), two low-recovery diodes ($D_p$ and $D_n$), and a fast diode (Do). However, the two power switches can be driven by the same control signal, which significantly simplifies the control circuitry. Moreover, the structure of the proposed topologies utilizes one additional inductor compared to the conventional topologies, which are often described as a disadvantage in terms of size and cost. However, better thermal performance can be achieved with the two inductors compared to a single inductor. This is because each power switch is operating during half-line period. On the other hand, the components voltage stresses are equal to their counterparts in the conventional SEPIC converter.

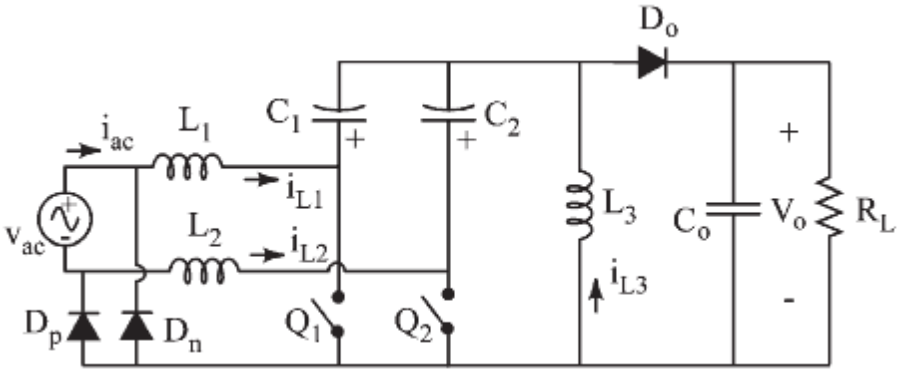


**Fig1: Bridgeless SEPIC PFC Rectifier**

### 3 . Principle Of Operation Of The Bridgeless Rectifier

The bridgeless rectifier shown in Figure 1 is constructed by connecting two DC–DC converters. Referring to Figure 1 during the positive half-line cycle, the first DC–DC SEPIC circuit $L_1$–$Q_1$–$C_1$–$L_3$–Do is active through diode Dp, which connects the input ac source to the output ground. During the negative half-line cycle, the second DC–DC SEPIC circuit, $L_2$–$Q_2$–$C_2$–$L_3$–$D_0$, is active through diode Dn, which connects the input ac source to the output ground. Thus, due to the symmetry of the circuit, it is sufficient to analyse the circuit during the positive half-period of the input voltage. The rectifier is operated when the switch Q1 is turned

on then diode Dp is forward biased by the sum inductor currents $i_{L1}$ and $i_{L2}$. As a result, diode $D_n$ is reversed biased by the input voltage. The output diode is reversed biased by the reverse voltage ($V_{ac}$ + $V_0$). Thus, the loss due to the turn-on switching losses and the reverse recovery of the output diode are considerably reduced. Equations for both rectifiers are identical, provided that the voltages on the capacitors for the SEPIC rectifier.

$$V_{c1}(t) = V_{c2}(t) + V_{ac}(t) = \begin{cases} V_{ac}(t); 0 \le t \le T/2 \\ 0 \quad ; \ T/2 \le t \le T \end{cases}$$

## 4. Modes Of Operation

The circuit operation during one switching period Ts in a positive half-line period can be divided into three distinct operating modes, as shown in Fig 2 to Fig 4, and it can be described as follows.

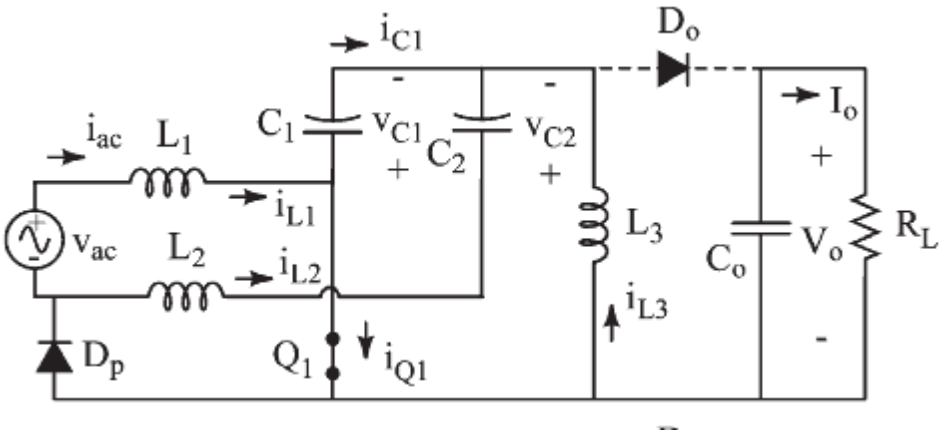


**Fig 2 : Switch Q1 ON Topology**

Mode 1 [$t_0$, $t_1$]

In this stage, the three-inductor currents linearly increase at a rate proportional to the input voltage *v*ac. The rate of increase of the three inductor currents is given by

$$\frac{di_{Ln}}{dt} = \frac{V_{ac}}{dt} \qquad n = 1,2,3$$

During this stage, the switch current is equal to the sum of the three inductors currents. Thus, the peak switch current $I_{Q1-pk}$ is given by

$$I_{Q1-pk} = \frac{V_m}{L_g} D_1$$

where,

$$\frac{1}{L_g} = \frac{1}{L_1} + \frac{1}{L_2} + \frac{1}{L_3}$$

Let $D_1$ be the duty cycle of switch $Q_1$. This interval ends when $Q_1$ is turned off, initiating the next subinterval.

Mode 2 [$t_1$, $t_2$]

At the instant $t_l$, switch $Q_1$ is turned off, diode Do is turned on, simultaneously providing a path for the three inductor currents. Diode $D_p$ remains conducting to provide a path for $iL_1$ and $iL_2$. In this stage, the three inductor currents linearly decrease at a rate proportional to the output voltage $V_o$. The three inductor currents are given by

$$\frac{dL_n}{dt} = \frac{-V_0}{L_n} \qquad n = 1,2,3$$

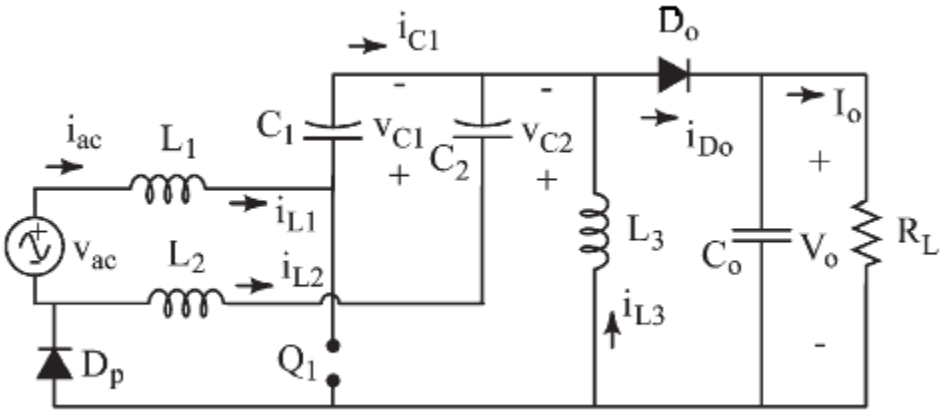


**Fig 3: Switch Q1 OFF Topology**

At the end of this mode the output diode current $i_{DO}$ smoothly reaches to zero and Do becomes reverse biased. The normalized length of this interval is given by

$$D_2 = \frac{D_1}{M} sin\omega t$$

Mode 3 [$t_2$, $t_s$]

In this stage, both $Q_1$ and $D_o$ are in their off-state. Diode $D_p$ provides a path for $i_{L3}$. The three inductors behave as current sources, which keeps the currents constant. Hence by end of this interval, the voltage across the three inductors is zero. Capacitor $C_1$ is charging up by $i_{L1}$, while $C_2$ is discharged by $i_{L2}$.

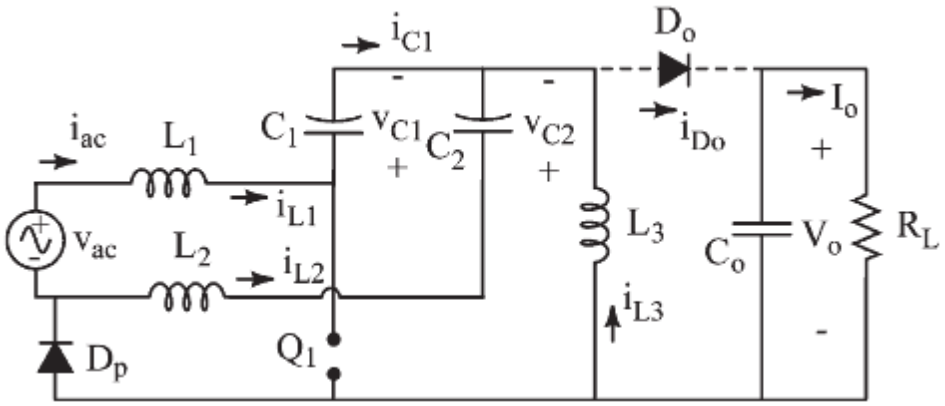

**Fig 4: DCM Topology, Solid And Dashed Lines Represent Active And Inactive Elements.**

## 5. Comparision Between Conventional And Bridgeless SEPIC PFC Rectifier

The circuit components in both the conventional PFC SEPIC rectifier and the improved bridgeless PFC SEPIC have similar peak voltage and current stresses. However, the bridgeless SEPIC is subjected to the input inductors ($L_1$ and $L_2$), the coupling capacitors ($C_1$ and $C_2$), and the active switches ($Q_1$ and $Q_2$) to a lower rms current stress compared to their counter parts in the conventional SEPIC topology. Moreover, the bridgeless SEPIC is constructed by connecting two DC–DC converters, each operating as SEPIC DC-DC converter, the switching performance of the two converters remains the same, which results in switching losses. Table 1 gives the comparison between conventional and bridgeless SEPIC PFC DCM based on the equipments and current conduction path.

**TABLE 1: Comparison Between Conventional And Bridgeless SEPIC PFC DCM Rectifier**

| ITEM | | Bridgeless SEPIC | conventional SEPIC |
|---|---|---|---|
| Slow diode | | 2 | 4 |
| Fast diode | | 1 | 1 |
| Switch | | 2 | 1 |
| Current conduction path | Stage1 | 1Slow diode 1Fast diode | 2Slow diodes, 1Switch |
| | Stage2 | 1Slow diode 1Fast diode | 2Slow diodes 1Fast diodes |
| | DCM | 1Slow diode | 2Slow diodes |

## 7. CONCLUSION

The single-phase bridgeless rectifiers with low input current distortion and low conduction losses have been presented. The bridgeless rectifier is derived from the conventional SEPIC converter. Comparing with conventional SEPIC and Power Factor Correction circuits, due to the lower conduction loss and switching loss, Bridgeless DCM SEPIC PFC rectifier topologies can further improve the conversion efficiency. To maintain same efficiency, the improved circuits could operate with higher switching frequency. Thus, additional reduction in the size of PFC inductor and EMI filter could be achieved. Besides improving circuit topology and performance, a further reduction in rectifier size could be realized by integrating the three inductors into a single magnetic core.

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