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SIMULATION OF NOVEL MAGNETIC TUNNEL JUNCTION FOR READ-WRITE PERFORMANCE IN IN-PLANE ANISOTROPY

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ABSTRACT

This Paper gives an investigation into simulation of novel magnetic tunnel junction for read write performance in in-plane anisotropy. Magnetic Tunnel Junction known as MTJ which is due to rise in spintronic result in becoming a novel memory. The occurrence geometry of the device for IPA devices is due to magneto crystalline effects. The switching characteristic is due to the thermal noise effect when the voltages is less than the critical switching voltage of the MTJ, and the switching characteristic is due to the spin torque transfer effect when the voltages is high than the critical switching voltage of the MTJ. In spin transfer torque magnetic tunnel junction, read disturbance play a vital role in read-write performance. This disturbance can be reduced by oxide thickness and the width of each transistor cell. Finally, simulation process in this study is done with verilog- A simulator. It is a subset of Verilog-AMS, easy to understand and global standardization.

KEYWORDS - Magnetic Tunnel Junction**,** Spintronic, Read Sense margin, In-plane Magnetic Anisotropy, Spin Transfer Torque

INTRODUCTION

In spin transfer torque magnetic tunnel junction, read-disturbance is the particular parameter that compromise in read-write performance. Read-disturbance is reduced by oxide thickness

and the width of each transistor cell. During the read operation, the probability, P_{WRITE}, of switching an MTJ, read sense current, I_{read} and the MTJ's critical current, I_{C0} is given by [1]:

$$P_{write} = 1 - \exp\left[- \frac{t_P}{\tau_{P \to AP}} \right]$$

(1)

Where t_p = time duration when $I_{read\ is}$ applied to the MTJ,

$\tau_{P \to AP}$ = switching time from parallel to anti-parallel state

Then switching time from parallel to anti parallel $\tau_{P \to AP}$ is given by:

$$\tau_{P \to AP} = \tau_0 \exp\left[\frac{VKu}{K_B T} \left(1 - \frac{I_{read}}{I_{CO}} \right) \right]$$

(2)

Where τ_0 = nominal switching time

K_u = parameter depends on the material composition and temperature

K_B = Boltzmann constant

T = temperature in Kelvin

V = volume of the layer

The above expression is very much helpful in reducing the read-disturbance.

From the above expression it is concluded that the read disturb rate is an exponentially increasing function of the ratio between the read sense current, I_{READ}, and the critical current, I_{C0}

The expression for Read sense margin which is denoted by RSM is given by

$$RSM = I_{read} \frac{R_{AP} - R_P}{2}$$

(3)

$$= I_{read} R_P \frac{TMR}{2}$$

(4)

Where

R_{AP} = MTJ in anti-parallel state resistance

R_P = MTJ in parallel state resistance

TMR = tunnel magnetic resistance

From the above expression, it is clear that MTJ in parallel state resistance, R_P is proportional to the read sense margin. The increase in oxide thickness results in increase in R_P. Thus it is concluded that the read sense margin is increased by increasing in oxide thickness. The increase in oxide thickness results in not only in increase in R_P but also it increase the TMR resistance[2,3].Since the read sense margin is directly proportional to the both MTJ resistance and the tunnelling resistance. The increase in oxide thickness results in two different ways in according to read-write performance and they are:

1. The increase in oxide thickness result in high speed read access
2. The increase in oxide thickness result in low speed write access

The second result is overcome with the increase in transistor cell width thickness. Since the increase in transistor cell width result in increase in read-write access time but it also has its disadvantages that the read performance is disturbed. Therefore a novel model is developed in our study to overcome the problem discussed.

During the read performance operation thermal stability play an important role in controlling the data storing capabilities. Thus thermal stability is also one of the parameter which affects the read-write performance. To reduce the low read disturb rate, the value of thermal stability is taken more than 55 [1]. The value of thermal stability is taken as 55 for 10 years data retention. The value of thermal stability is expressed as Δ and given by

$$\Delta = \frac{K_u V}{K_B T} \quad (5)$$

Where

$$K_U = \frac{M_s H_K}{2}$$

(6)

Where M_S = saturation magnetization

H_K = effective anisotropy field

The smaller value of thermal stability results in decrease in critical current because thermal stability is proportional to the magnetostatic potential energy. The relationship between critical current and the thermal stability of **in plane magnetic anisotropy** is expressed as

$$I_{CO} = \frac{2e\alpha M_s V\left(H_K + 2\Pi M_s\right)}{\hbar\eta}$$

(7)

Where e = an elementary charge $1.6*10^{-19}$ C

α = Gilbert damping coefficient

ħ = plank constant

η = spin polarization factor

The above expression concluded that except M_s and H_k all the parameter are universal constant. Thus the critical current depends on the parameter M_s and H_k.

Modelling language

The choices of modelling language play an important role in compact modelling for the use of accurate, fast, efficient and easy modelling. There are various modelling language used such as Verilog A, C and FORTRAN, VHDL- AMS, Mat lab. Each one of these has its advantages and disadvantages

VHDL-AMS- This modelling is very fast, accurate but it is used in limited simulator and it is harder to simulate quickly

MATLAB- It is a good fitting data but it is unable to run alone

VERILOG- A- It is a subset of Verilog-AMS. It is easy to understand. It is global standardization. It can run in AMS simulator Spectre, ELDO, ADS. It is one of the HDL languages.

Previous work done in designing memory cell model

There are many proposed models for MTJ have been developed but each of them has its advantages and disadvantages in correlation to measured data. The first model developed by

Young Min Lee [4]. In our study this model will be recognized by conventional cell model.The second model developed by Jing Li et al. [5]. In this model 2-transistor 1 magnetic tunnel junction STT- MRAM cell is used. The main restriction in this model is that it make less intense on read disturbance which means in this model read performance is not improved while maintaining the disturbance free read operation. To overcome this problem separate read and write operation have been proposed [6, 7].The second model developed by the N.N. Mojumder et al. [7]. In this model 3- transistor 1 magnetic tunnel junction STT-MRAM is used. Since in this model separate read and write operation is used therefore read and write access is independently optimized.

Device proposed model:

Our model is based on 3- transistor 1 magnetic tunnel junction STT-MRAM. Parameter of the materials were chosen to compare the characteristics of conventional cell with propose cell. The various MTJ parameters used are detailed below in Table: 1

Table:1
MTJ parameters for IPA Devices

S. No	Data	Value	Unit
1	Saturation magnetization, M_s	1050	emu/ cm^3
2	Thermal stability factor, Δ	55 for conventional cell	no unit
		41 for proposed cell	
3	Gilbert damping constant, α	0.001	no unit
4	Critical current density, J_{CO}	2.2	MA/cm^3

.

Device Optimization

The size of transistor cell and the thickness of the oxide layer play a vital role in performance and the efficiency in read write application. In read write application the time taken to read operation is 50% and the time taken to write operation is 50%. Thus it can be expressed as

$$T_{AVERAGE}^{50-50} = 0.5T_{READ} + 0.5T_{Write} \quad (8)$$

Two results obtained in increasing the oxide layer thickness and they are: the switching time is also increased while increasing the oxide layer thickness because the oxide layer thickness is exponentially proportional to tunnelling barrier resistance and thus decreases the amount of current provided to the device.

Read sense current is also increased while increasing the oxide layer thickness. Thus, in our study, we obtained the value which decreases $T_{AVERAGE}^{50-50}$

Fig: 1 show the plot between the thickness of the oxide and the average operation time in IPA devices and fig: 2 show the relationship between the transistor cell size and the average operation time in IPA devices.

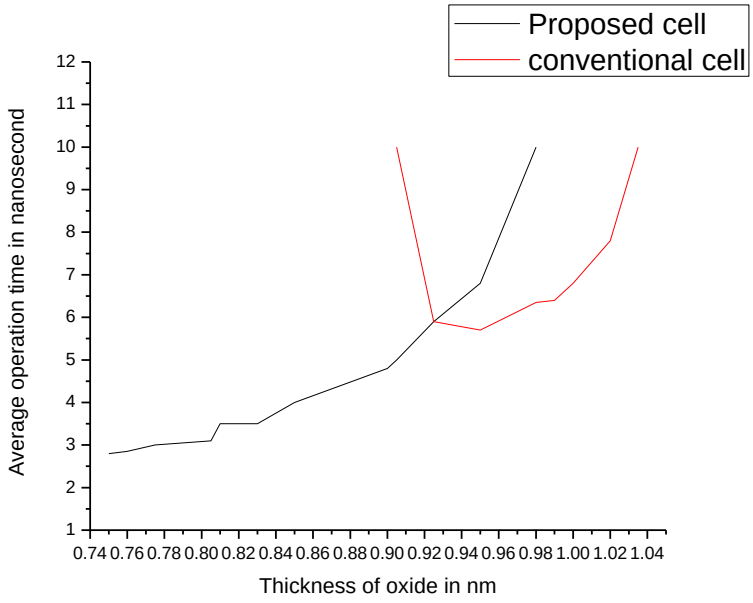

Fig: 1 Representation of thickness of oxide versus average operation time in IPA devices

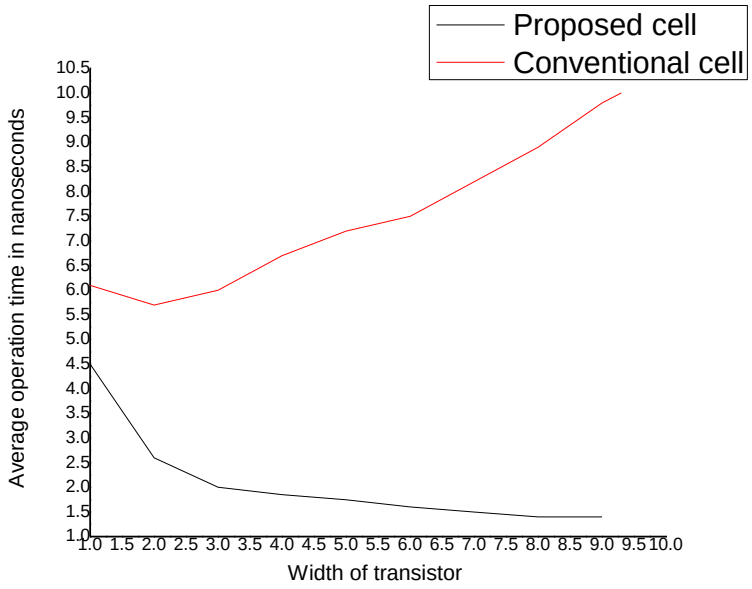

Fig: 2 Representation of thickness of oxide versus average operation time in IPA devices

Result: Model correlation

In our correlation, the fig: 1 concluded that the average operation time is monotonically increasing with width of transistor in our proposed model whereas conventional model is non monotonically increasing with width of transistor and fig: 2 concluded that the average operation time is monotonically decreasing with width of transistor in our proposed model whereas conventional model is non monotonically decreasing with width of transistor.

Conclusions

A new type of simple novel magnetic tunnel junction for read write performance in in-plane anisotropy is presented. We propose and computationally analysis the read-write performance of MTJ. The curve fitting of this model is more accurate to obtain good result.

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